

Notice of References CitedApplication/Control No.
09/288,263Applicant(s)/Patent Under
Examination
WAKI ET AL.Examiner
Christian La ForgiaArt Unit
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,170,083	01-2001	Adl-Tabatabai, Ali-Reza	717/158
	B	US-6,151,618	11-2000	Wahbe et al.	709/1
	C	US-6,301,652	10-2001	Prosser et al.	712/204
	D	US-6,044,222	03-2000	Simons et al.	717/156
	E	US-5,923,883	07-1999	Tanaka et al.	717/156
	F	US-6,381,739	04-2002	Breternitz et al.	714/37
	G	US-5,836,014	11-1998	Faiman, Jr., Robert Neil	717/156
	H	US-5,724,590	03-1998	Goettelmann et al.	717/154
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Leung, Allen et al. Run-time versus Compile-time Instruction Scheduling in Superscalar (RISC) Processors: Performance and Tradeoffs. 1996. IEEE. p. 215-224.
	V	B. Natarajan et al. Spill-Free Parallel Scheduling of Basic Blocks. 1995. IEEE. p. 119-124.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.